WEST Search History

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DATE: Tuesday, October 26, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L28	l6.clm. and L22	17
☐	L27	l6.ab. and L22	2
☐	L26	l6 and L22	76
☐	L25	l15.clm. and L22	0
☐	L24	l15.ab. and L22	0
☐	L23	l16 and L22	14
☐	L22	l19 or l20 or L21	2080
☐	L21	307/31.ccls.	375
☐	L20	713/320,323.ccls.	980
☐	L19	713/300,310.ccls.	1077
☐	L18	(power adj management) same port same (protocol near2 availabl$7)	1
☐	L17	(power adj management) with port with protocol	2
☐	L16	(power adj management) same port same protocol	70
☐	L15	(power near3 manag$7) same port same protocol	77
☐	L14	l6 same acknowledg$7	10
☐	L13	L12 same response	1
☐	L12	L11 same request$4	1
☐	L11	(power adj management adj state adj transition)	8
☐	L10	l6 same L8	1
☐	L9	l6 and L8	17
☐	L8	(first near3 device) same (second near3 device)	124151
☐	L7	L6 same (state near3 transition)	6
☐	L6	(power near3 manag$7 near3 request$4)	192
☐	L5	l3 and (power$4 near3 manag$7)	2
☐	L4	L3 same power$4	0
☐	L3	(first adj DSL) same (second adj DSL)	23
☐	L2	(DSL with peers)	1
☐	L1	(DSL adj peers)	0

END OF SEARCH HISTORY

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

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L2: Entry 1 of 1 File: USPT Mar 30, 1999

DOCUMENT-IDENTIFIER: US 5889470 A
**** See image for Certificate of Correction ****
TITLE: Digital subscriber line access device management information base

Detailed Description Text (10):
The preferred embodiment of enterprise DSL MIB 29 of the present invention allows network management of DSL access devices in two modes of operation. In synchronous mode, management station 14 communicates with SNMP agent 23 on DSL access concentrator device 12, across network 16, indicating which DSL access device 21 or DSL interface 25 is to be accessed. SNMP agent 23 acquires information from enterprise DSL MIB 29. Alternatively, SNMP agent 23 uses sub agent 27 to contact a corresponding sub agent peer 28 located on DSL access device 21. In this manner, SNMP agent 23 acts as a proxy for a selected DSL access device 21, and is considered to be operating in synchronous mode.

Detailed Description Text (11):
In asynchronous mode, sub agent 28 on DSL access device 21 operates independently of SNMP agent 23. In this mode, SNMP agent 23 merely accesses enterprise DSL MIB 29, using the latest available information. Sub agent peer 28, based upon predefined policies internal to DSL access concentrator device 12, acquires information from DSL access device 21, and updates enterprise DSL MIB 29 via line 24. In this manner, SNMP agent 23 still acts as a proxy for a selected DSL access device 21, but the operation is considered to be asynchronous.

Previous Doc Next Doc Go to Doc#

L5: Entry 1 of 2 File: USPT Oct 12, 2004

DOCUMENT-IDENTIFIER: US 6804292 B2
TITLE: Broadband I/O circuits, interface and bus

Brief Summary Text (24):
Another aspect of the present invention includes the use of an improved protocol for exchanging operational and/or control information between separated digital and analog sections of an xDSL modem. This operational and/or control information preferably includes information relating to real time control settings for circuits located within the analog codec, power management, and the like.

Detailed Description Text (27):
(4) power management information, such as an ADSL wake-up signal, or a power loss signal received by DSL Digital IC 230 from the motherboard. The power loss signal from the motherboard, in the case of ADSL, is used by DSL Modem Digital Controller 230 for generating a dying gasp message to be transmitted to a remote transceiver through DSL Modem Analog Circuit 205. Other types of control information associated with a conventional xDSL link can also be accommodated.

Detailed Description Text (33):
To achieve this variable number of channels capability, a frame structure for the word clock cycles is illustrated in FIG. 3C. As illustrated, a certain number M (programmable by software and set to a value of 2 as shown) of word clock cycles forms a frame clock to support M separate DSL channels (or separate analog circuits) in each direction. It is unnecessary, of course, for all M channels to be active at one time. To mark the beginning of a frame, the word clock is held high for a duration of two clock cycles. At startup, M is initially set to 1. To operate with multiple channels, DSL Digital IC 230 passes a control signal via the EOC noted earlier, to set M to some higher integer value in the DSL Modem Analog Circuit 205, such as M=2. A multi-channel frame is then indicated by WORD CLOCK being set high for two clock cycles. As depicted in FIG. 3C, the data for channel 2 (or the second DSL Modem analog circuit) is presented at the beginning of the frame cycle (i.e., when WORD CLOCK is high for two cycles) and the data for channel 1 (or the first DSL Modem analog circuit) is presented during the second half of the frame cycle (during the time WORD CLOCK is high for a single cycle). Thus, in the multi-channel data frame of FIG. 3C, there are two data channels, and data is transferred through a first channel during a first time period of the multi-channel data frame, and through a second channel during a second time period of the multi-channel data frame.

CLAIMS:

18. The protocol of claim 17, wherein said operational and/or control information further includes information relating to power management for an xDSL modem.

30. The digital controller of claim 26, wherein said transmit control signals relate to power management for the broadband modem.

35. The codec of claim 32, wherein said control information relates to power management operations to be performed by the broadband modem.

L5: Entry 2 of 2 File: USPT Feb 5, 2002

DOCUMENT-IDENTIFIER: US 6345072 B1
TITLE: Universal DSL link interface between a DSL digital controller and a DSL codec

Brief Summary Text (24):
Another aspect of the present invention includes the use of an improved protocol for exchanging operational and/or control information between separated digital and analog sections of an xDSL modem. This operational and/or control information preferably includes information relating to real time control settings for circuits located within the analog codec, power management, and the like.

Detailed Description Text (27):
(4) power management information, such as an ADSL wake-up signal, or a power loss signal received by DSL Digital IC 230 from the motherboard. The power loss signal from the motherboard, in the case of ADSL, is used by DSL Modem Digital Controller 230 for generating a dying gasp message to be transmitted to a remote transceiver through DSL Modem Analog Circuit 205. Other types of control information associated with a conventional xDSL link can also be accommodated.

Detailed Description Text (33):
To achieve this variable number of channels capability, a frame structure for the word clock cycles is illustrated in FIG. 3C. As illustrated, a certain number M (programmable by software and set to a value of 2 as shown) of word clock cycles forms a frame clock to support M separate DSL channels (or separate analog circuits) in each direction. It is unnecessary, of course, for all M channels to be active at one time. To mark the beginning of a frame, the word clock is held high for a duration of two clock cycles. At startup, M is initially set to 1. To operate with multiple channels, DSL Digital IC 230 passes a control signal via the EOC noted earlier, to set M to some higher integer value in the DSL Modem Analog Circuit 205, such as M=2. A multi-channel frame is then indicated by WORD CLOCK being set high for two clock cycles. As depicted in FIG. 3C, the data for channel 2 (or the second DSL Modem analog circuit) is presented at the beginning of the frame cycle (i.e., when WORD CLOCK is high for two cycles) and the data for channel 1 (or the first DSL Modem analog circuit) is presented during the second half of the frame cycle (during the time WORD CLOCK is high for a single cycle). Thus, in the multi-channel data frame of FIG. 3C, there are two data channels, and data is transferred through a first channel during a first time period of the multi-channel data frame, and through a second channel during a second time period of the multi-channel data frame.

CLAIMS:

19. The protocol of claim 18, wherein said operational and/or control information further includes information relating to power management for an xDSL modem.

41. The digital controller of claim 37, wherein said control signals relate to power management for the xDSL capable modem.

L7: Entry 2 of 6 File: USPT Jul 29, 2003

DOCUMENT-IDENTIFIER: US 6601179 B1

**** See image for Certificate of Correction ****

TITLE: Circuit and method for controlling power and performance based on operating environment

Detailed Description Text (42):

In the case where the transition is to a higher power state than before, an interrupt is made requesting control of power management to be passed to the micro-controller, which is now responsible for controlling operating characteristics, in this case an increase of supply voltage and operating frequency (Steps 520 and 525). First, the micro-controller signals the voltage control circuit to program the power supply circuit to increase the supply voltage to an appropriate level prescribed for the higher power state (Step 530). This increase in the supply voltage is applied immediately. Next, the micro-controller signals the frequency control circuit to increase the operating frequency of the processor to an operating frequency prescribed for the higher power state by loading a particular bus ratio (Step 535). However, this increase is not applied until after the processor is reset.

Detailed Description Text (44):

In the case where the transition is to a lower power state, an interrupt is made requesting control of the power management to be passed to the micro-controller (Steps 555 and 560). The micro-controller signals the frequency control circuit to decrease the operating frequency of the processor to a prescribed operating frequency (Step 565). This is accomplished by initially storing processor state information, and thereafter, resetting the processor and loading a reduced bus ratio through activation of CPURST# and CRESET# signals, respectively (Steps 570 and 575). As a result, the bus ratio corresponding to the decreased operating frequency is loaded into the processor.

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L7: Entry 3 of 6 File: USPT Sep 3, 2002

DOCUMENT-IDENTIFIER: US 6446214 B2
** See image for Certificate of Correction **
TITLE: System and method for handling power state change requests initiated by peripheral devices

Abstract Text (1):
A computer operating system is coupled to intelligent peripheral devices via a peripheral bus architecture that supports unsolicited status requests from peripheral devices. Each peripheral device has local power management that initiates an unsolicited power change request when the device is preparing to change power states. The peripheral bus carries the unsolicited power change request to the operating system. Upon receipt, the operating system issues a power change request directing the peripheral device to perform the power state transition. In this manner, the operating system remains aware of the peripheral device's power state and acts as if it is controlling the device's power state transitions.

Brief Summary Text (13):
When the local power management decides to change power states, the local power management initiates an unsolicited power change request indicating a new power level. The peripheral bus carries the unsolicited power change request to the operating system. Upon receipt of the unsolicited power change request, the operating system issues a power change request directing the peripheral device to perform the power state transition. In this manner, the operating system remains aware of the peripheral device's power state and in fact, acts as if it is controlling the device's power state transitions.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L7: Entry 5 of 6 File: USPT Nov 25, 1997

DOCUMENT-IDENTIFIER: US 5692204 A
TITLE: Method and apparatus for computer system power management

Brief Summary Text (7):
Other prior art solutions use a cooperative approach wherein hardware communicates, via system firmware, with a central power management executive in the operating system to manage the power state of system devices. An example of this approach is the Advanced Power Management (APM) provided by Intel Corporation and Microsoft Corporation and the various operating systems, such as Windows (trademark of Microsoft Corp.) and OS/2 (trademark of IBM Corp.), which employ APM. In this approach both system firmware and specifically enabled power management-aware applications communicate with a central power management executive. Power management event notification messages are passed up from devices through the power management extended system firmware to the power management executive and requests for system power state transitions are passed down from the applications software. This provides a more adaptive approach to power management, but still involves many trade-offs between reduced power consumption and reduced resource availability.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L11: Entry 1 of 8 File: USPT Jun 10, 2003

DOCUMENT-IDENTIFIER: US 6577856 B1
TITLE: System and method for performing power management without losing data, connectivity or reachability

Detailed Description Text (5):
The EOC handshake is used for power management coordination between the ATUs. The EOC handshake ends in either a successful or unsuccessful result. If the result is successful, it is a grant event which is used to enable a power management state transition. If the EOC handshake ends in an unsuccessful result, a state transition is not triggered and the power management state is unchanged. The EOC handshake procedure includes a sequence of EOC commands. If any of the EOC command, read or write protocols used in the EOC handshake detects an EOC protocol error condition, the EOC handshake terminates and the result is unsuccessful.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L11: Entry 2 of 8 File: USPT Sep 3, 2002

DOCUMENT-IDENTIFIER: US 6446215 B1
TITLE: Method and apparatus for controlling power management state transitions between devices connected via a clock forwarded interface

Abstract Text (1):
A method and apparatus for controlling power management state transitions between two devices, e.g., a processor and a bus bridge, that are connected through a clock forwarded interface bus in a computer system. The bus bridge is configured to coordinate disconnection of the processor from the interface. Particularly, the bus bridge may use a fist signal to indicate whether or not the processor is to be disconnected from the interface (e.g. a CONNECT signal) and the processor may use a second signal to indicate whether or not the processor is to be disconnected from the interface (e.g. a PROCREADY signal). The processor is disconnected from the interface responsive to both the first signal and the second signal indicating that the processor is to be disconnected. The signals may also be used to reconnect the processor to the interface.

Detailed Description Text (63):
The foregoing discloses a method and apparatus for controlling power management state transitions between two devices (here, a processor and a bus bridge) that are connected through a clock forwarded interface bus in a computer system. The disconnection of the processor from the interface bus (for example, to save power consumption by the processor) may be accomplished through a logical connection-disconnection protocol implemented between the processor and the bus bridge and without burdening the processor to monitor the interface bus for activity. The combination of CONNECT, PROCREADY and CLKFWDRESET signals allow the processor and the bus bridge to accomplish processor disconnection and reconnection without jeopardizing the integrity of the clock forwarded interface. Broadly speaking, forward clocks and any associated data are consistently transmitted between two devices (here, a processor and a bus bridge) in a deterministic manner.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L11: Entry 5 of 8 File: USPT Jun 9, 1998

DOCUMENT-IDENTIFIER: US 5765001 A
TITLE: Computer system which is operative to change from a normal operating state to a suspend state when a power supply thereof detects that an external source is no longer providing power to said power supply at a predetermined level

CLAIMS:

28. The computer system of claim 27, wherein said code is BIOS code characterized by implementing power management state transitions and monitoring the state of said control signal, said BIOS code being capable of interrupting the execution of other code on the CPU and executing said suspend routine in response to said power supply activating said control signal.

29. The computer system of claim 27, wherein said code is operating system code characterized by controlling power management state transitions, said operating system code capable of interrupting the execution of other code on the CPU and calling said suspend routine in response to said power supply activating said control signal.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L14: Entry 1 of 10 File: USPT Oct 5, 2004

DOCUMENT-IDENTIFIER: US 6802014 B1
TITLE: Method and apparatus for managing power in computer systems

Detailed Description Text (41):
FIGS. 10 and 11 illustrate the power-down-on-request procedure used in some embodiments of the invention. As further described below, in such a procedure, the power-down request propagates down that power manager object hierarchy, and the power-down acknowledgments propagate up this hierarchy.

Previous Doc Next Doc Go to Doc#

L14: Entry 2 of 10 File: USPT Mar 23, 2004

DOCUMENT-IDENTIFIER: US 6711691 B1
TITLE: Power management for computer systems

Detailed Description Text (65):
The shutdown processing 1000 then determines 1016 whether the quiescent acknowledgements (QACKs) have been asserted. Once the decision 1016 determines that the quiescent acknowledgement (QACK) has been asserted, the last active processor enters 1018 a sleep mode. Here, all other processors are already in the sleep mode. Thereafter, the memory controller/bus manager and the I/O interrupt controller (IOIC) begin 1020 an internal shutdown sequence. The shutdown processing 1000 then determines 1022 whether the suspend acknowledgements (SUSACK1, SUSACK2) have been asserted. Here, the shutdown processing 1000 awaits the reception of the suspend acknowledgement (SUSACK1) from the memory controller/bus manager and the suspend acknowledgement (SUSACK2) from the I/O-interrupt controller to indicate that their respective internal shutdown sequences have been completed. Once the suspend acknowledgements (SUSACK1, SUSACK2) have been received, the power manager stops all clocks, asserts processor resets, and removes power to the processors at 1024. Then, the shutdown processing 1000 determines 1026 whether the off was requested and used to invoke the shutdown processing 1000. When it is determined 1026 that off has been requested, then the power manager asserts all resets and removes all power at 1028. In this case, the computer system is placed in the off state 202 and the shutdown processing 1000 is complete and ends. On the other hand, when it is determined 1026 that off has not been requested (i.e., sleep requested), then the computer system is placed in the sleep all 212 state and the shutdown processing 1000 is complete and ends. In the sleep all state, the processors do not receive power, but the power manager, the DRAM and the various controllers continue to receive power so that the sleeping processors can be awakened as needed. However, the DRAM and the various controllers are typically also in a low power mode.

L14: Entry 3 of 10 File: USPT Dec 16, 2003

DOCUMENT-IDENTIFIER: US 6665520 B2
TITLE: Power management method of and apparatus for use in a wireless local area network (LAN)

Detailed Description Text (17):
The Control Point will respond to a Power Management Service Request message in the Control Point Beacon. If a station transmits a Power Management Service Request message and does not receive an acknowledgement in the next Control Point Beacon, it should repeat the Power Management Service Request up to a predetermined number of times or until an acknowledgement is received in the Control Point Beacon.

Detailed Description Paragraph Table (3):
Flag Name Description Power Saving Set: Registration as a PS station was Registration Flag successful. Station can now use PS capabilities. Power Saving Set: Power Management Service Request Denial Flag message received and PS services denied by the CP but, acknowledges that a Power Management Service End message was received from the station. Wake-up Flag Set: When it receives the CPB the addressed station should come out of power-save mode, broadcast a Power Management Status message and remain awake. Clear: No action required. Wake-up Request Set: A Power Management Service Request Acceptance Flag message containing a wake-up request was received from the station and was accepted. Wake-up Request Set: A Power Management Service Request Denial Flag message containing a wake-up request was received from the station but was rejected.

L14: Entry 4 of 10 File: USPT Jul 1, 2003

DOCUMENT-IDENTIFIER: US 6587950 B1
** See image for Certificate of Correction **
TITLE: Cluster power management technique

Brief Summary Text (13):
A power management technique for a cluster having a group of hosts connected to a group of I/O (input/output) units via a cluster interconnection fabric includes: transmitting an OS (operating system) independent power management request from a Cluster Power Manager to an OS Power Manager within one of the hosts via a Control Element in the host and the fabric. A reply to the request from the Control Element is transmitted to the Cluster Power Manager via the fabric. A command to the Control Element is transmitted from the Cluster Power Manager via the fabric. The command from the Control Element is transmitted to the OS Power Manager and an I/O Controller Device Driver Stack in the host. A command completion acknowledgment is transmitted from the Control Element to the Cluster Power Manager via the fabric.

CLAIMS:

1. A method of power management for a cluster comprising a plurality of hosts connected to a plurality of I/O (input/output) units via a cluster interconnection fabric, the method comprising: transmitting an OS (operating system) independent power management request from a cluster power manager to an OS power manager within one of the hosts via a control element in the host and the fabric; transmitting a reply to the request from the control element to the cluster power manager via the fabric; transmitting a command to the control element from the cluster power manager via the fabric; transmitting the command from the control element to the OS power manager and an I/O controller device driver stack in the host; and transmitting a command completion acknowledgment from the control element to the cluster power manager via the fabric.

19. A computer program product comprising: a computer usable medium having a computer readable program code means embodied in said medium for power managing a cluster comprising a plurality of hosts connected to a plurality of I/O (input/output) units via a cluster interconnection fabric, said computer program product comprising: a computer readable program code means for causing a transmission of an O/S (operating system) independent power management request from a cluster power manager to an O/S power manager within one of the hosts via a control element in the host and the fabric; a computer readable program code means for causing a transmission of a reply to the request from the control element to the cluster power manager via the fabric; a computer readable coding means for causing a transmission of a command to the controller element from the cluster power manager via the fabric; a computer readable program code means for causing a transmission of the command from the control element to the O/S power manager and an I/O controller device stack in the host; and a computer readable program for causing a transmission of a command completion acknowledgment from the control element to the cluster power manager via the fabric.

20. A computer-readable medium that stores computer-executable instructions, the computer-executable instructions, when executed, causing a computer to: receive an OS (operating system) independent power management request from a cluster power